Understanding I2S Bus and Audio Isolation

Generic background — how digital audio links work and why you might isolate them. No product ordering codes.

Document version · revised

1. Noise and galvanic isolation

Fast digital circuits, switch-mode supplies, and shared grounds often couple noise into sensitive audio paths — hum, buzz, or fuzzy ADC captures. **Galvanic isolation** breaks the direct current path between two boards while still letting selected digital signals cross through isolator ICs.

Isolation boards (such as Turul I2S-001) are one way to keep a noisy processor domain separate from an ADC/DAC/codec domain. This document explains the *signals* you count before choosing hardware — not a specific bill of materials.

2. Digital side and audio side

Digital side — MCU, SoC, or FPGA: digital I/O only on that chip (no analog audio I/O).

Audio side — ADC, DAC, or codec: includes analog front-end circuitry you usually want quiet. Count how many **digital wires** cross between the two sides (ignore power/ground):

- **Toward audio side** — driven digital → converter (e.g. `BCLK`, `LRCK`, DAC data).
- **Back toward digital side** — driven converter → digital (e.g. ADC data, or clocks if the codec is master).

When the processor is I2S clock master, both clock lines usually count **toward audio**. When the codec is master, those clocks count **back toward digital** instead.

3. I2S bus configurations

I2S links one **clock master** and one **clock slave**. The master drives `BCLK` and `LRCK` / `WS`. Identify who is master in your design and whether you need one-way or duplex data.

Digital side is I2S clock master (Figures 1–3)

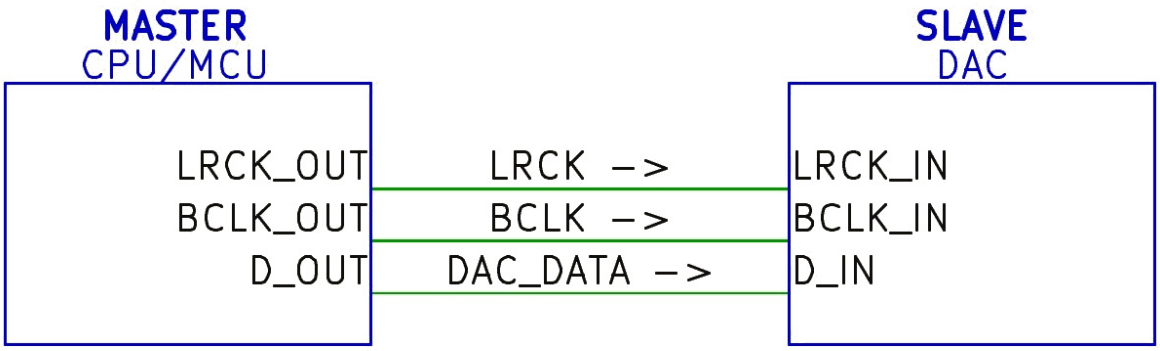

Figure 1. Master CPU/MCU → slave DAC — LRCK and BCLK out; DAC data toward the converter.

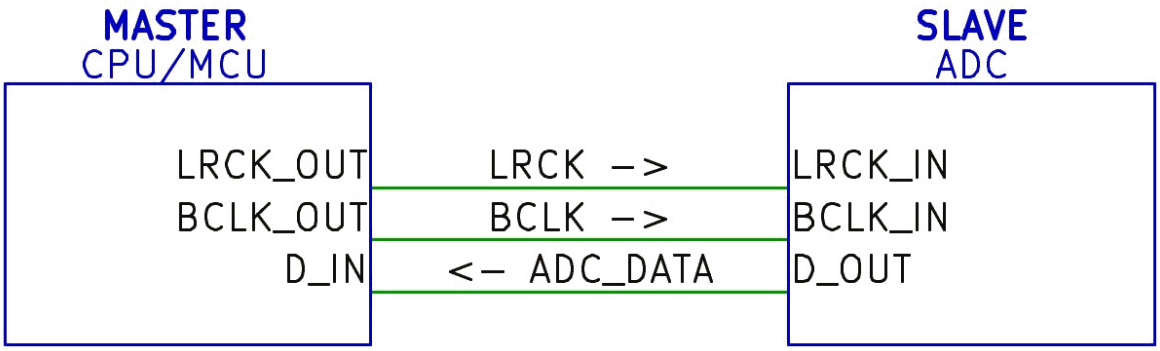

Figure 2. Master CPU/MCU ← slave ADC — LRCK and BCLK out; ADC data from the converter.

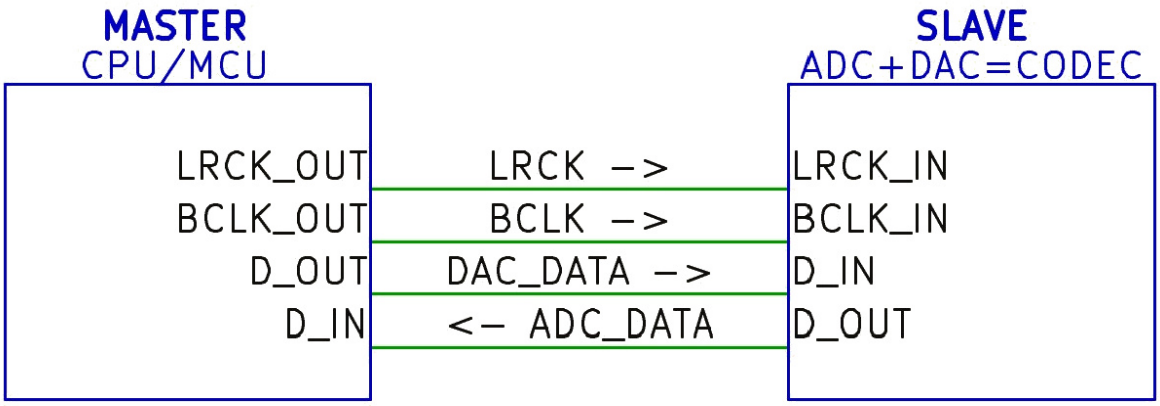

Figure 3. Master CPU/MCU ↔ slave CODEC — duplex ADC and DAC data.

Figure	Toward audio	Back to digital
1	**3**	**0**
2	**2**	**1**
3	**3**	**1**

Audio side is I2S clock master (Figures 4–6)

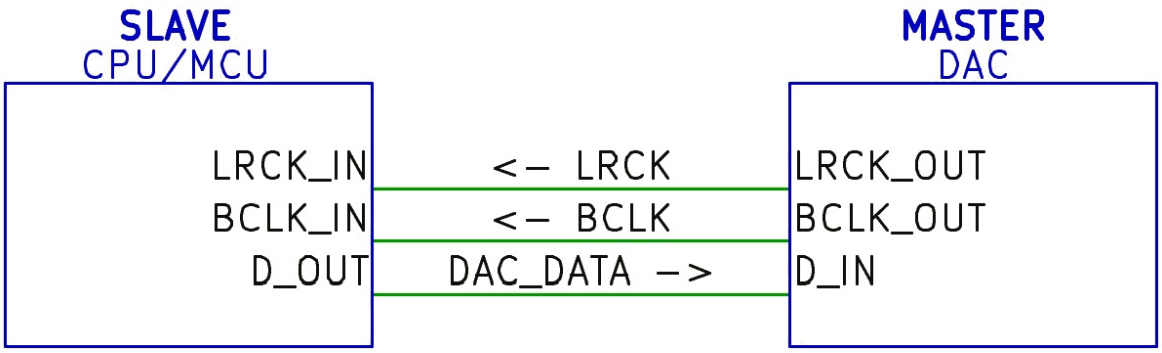

Figure 4. Slave CPU/MCU ← master DAC — DAC is clock master.

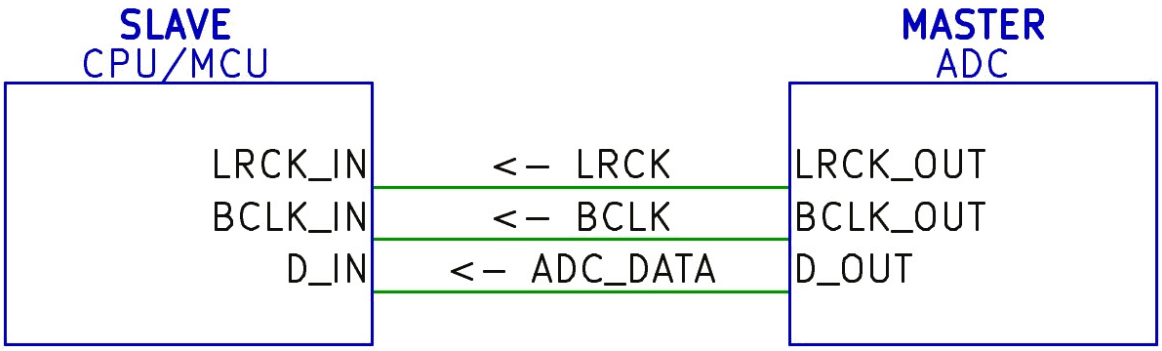

Figure 5. Slave CPU/MCU ← master ADC — ADC is clock master.

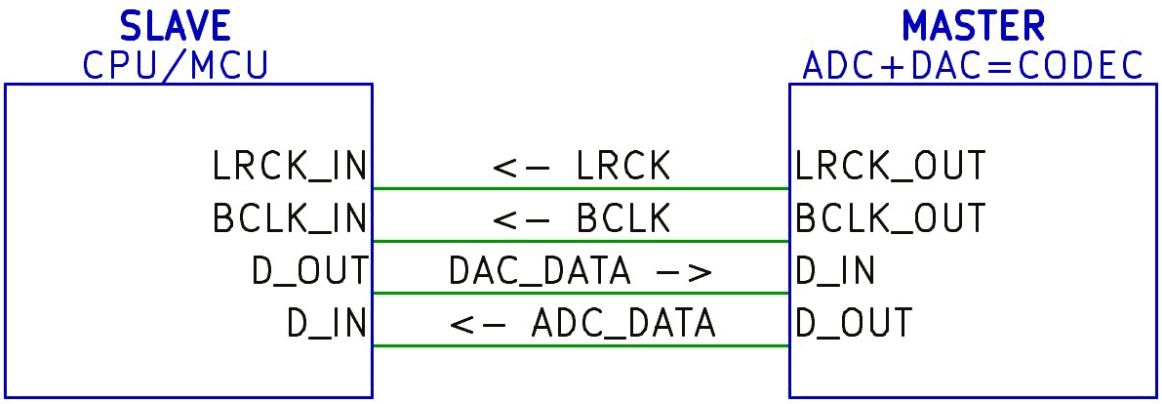

Figure 6. Slave CPU/MCU ↔ master CODEC — codec is clock master, duplex.

Figure	Toward audio	Back to digital
4	**1**	**2**
5	**0**	**3**
6	**1**	**3**

4. Master clock (MCLK)

Many codecs want a separate `MCLK` in addition to `BCLK` and `LRCK`. Your system may leave it unused, drive it from the MCU, or use a local oscillator on one of the boards.

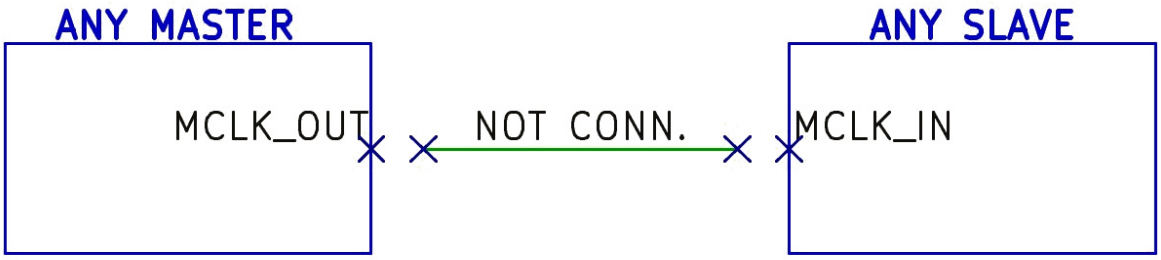

Figure 7. MCLK not connected — each side uses its own source or leaves MCLK unused.

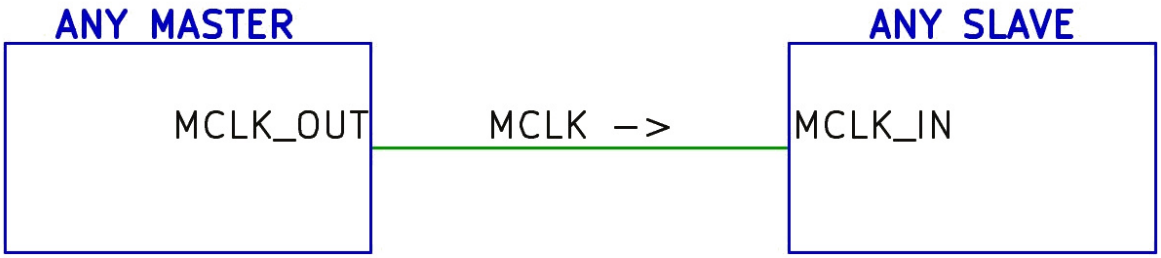

Figure 8. MCLK routed from one side toward the other in your system.

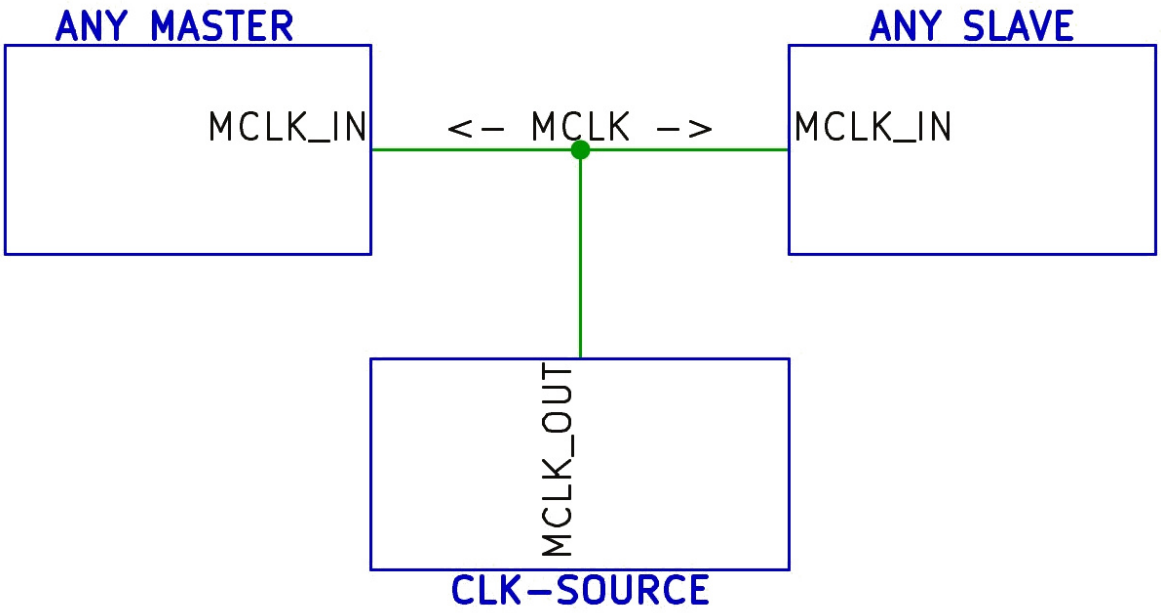

Figure 9. External CLK-SOURCE on your PCB feeds MCLK to master and slave.

Check your codec datasheet for required MCLK frequency and whether it must stay related to sample rate.

5. Extra control lines

Reset, data-ready, mute, and similar signals often ride alongside I2S. Count them the same way — toward audio vs back toward digital — when planning isolation.

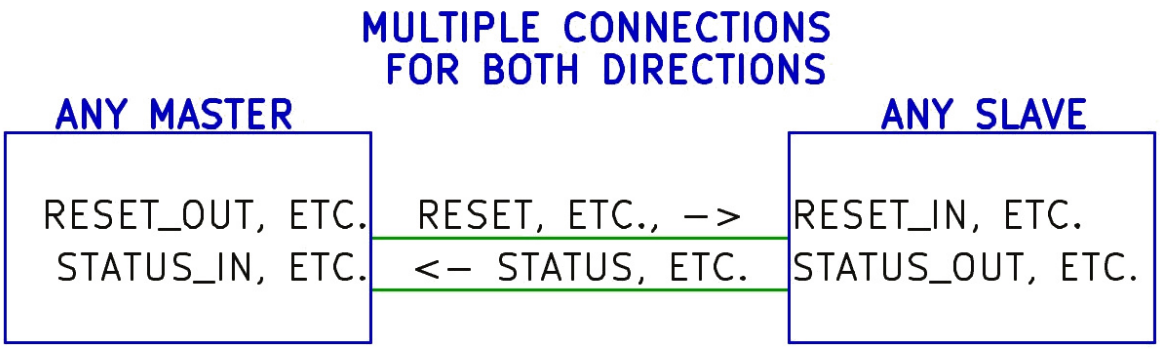

Figure 11. RESET toward the slave; STATUS back toward the master.

6. Typical power rails

Many hobby and module builds run **5 V** in and **3.3 V** I/O on MCU and codec from the same converted rail — an assumption only, not every product. An isolation board may use **separate supplies** on each side of the barrier (for example user dual supply or 5 V in with 3.3 V generated on the isolated side) — see the I2S-001 User's Guide for factory power options.

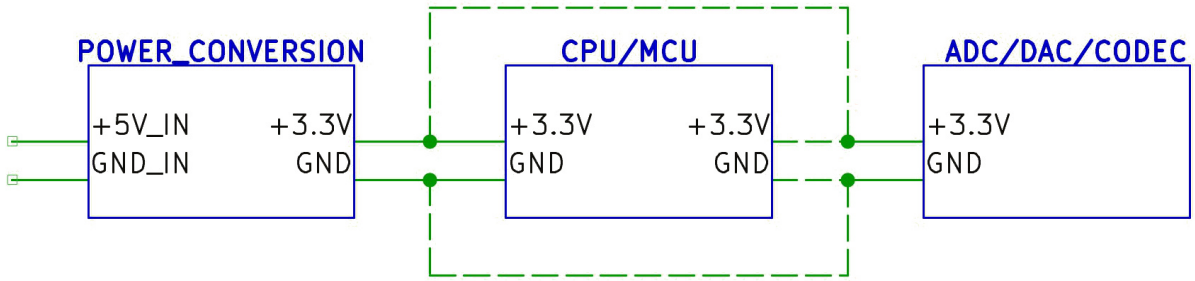

Figure 12. Typical module power — generic example; not I2S-001 pinout or ordering.