User's Guide

`I2S-001-ABCD`

Factory-configured part number — four digits **A**, **B**, **C**, **D** after the base SKU (e.g. **I2S-001-1101**). Pinout, wiring, and factory options.

Document version · revised

1. The board in 2 minutes

I2S-001 sits between your **digital side** and **audio side**. On the PCB, `J2` faces the digital side (silkscreen may say CPU or NOISY) and `J1` faces the audio / isolated side (codec). Each header exposes **12 pins** on a **2.54 mm** grid; pin *n* on `J2` pairs with pin *n* on `J1`. Power is on pins 5–6.

The board routes I2S clocks and data (and optionally I²C and extra GPIO) through galvanic isolation so ground loops and digital switching noise on the processor side are less likely to show up as hum or buzz on the analog audio path. Some of the parts can survive a kilovolt-class isolation rating; the **product** was not designed for that. Keep both sides at roughly the same potential — the barrier is there so the supplies and the signal wires do not carry noise across, not so you can stand off high voltage between domains.

If silkscreen on the board disagrees with this guide, **this guide wins**.

2. Pick your part number

Order the board as **`I2S-001-ABCD`**. Each digit is a factory option. The board is built to that code; you do not change **A**, **B**, **C**, or **D** after delivery. Example of the format: **`I2S-001-1101`**.

Digit	0	1	2
A — power	You supply both sides	**3.3 V** noisy in → isolated **3.3 V** out	**5 V** noisy in → isolated **3.3 V** out
B — I2S channels	Base **3 + 1** on pins 1–4	**4 + 4** on pins 1–4 and 7–10	—
C — pin 10	Your signal (GPIO, external `MCLK`, …)	On-board **12.288 MHz** on pin 10 of both headers	—
D — I²C isolator	No I²C on the board	`SDA` / `SCL` on pins 11–12	—

Digit **C** applies when **B = 1** — a board with **B = 0** and **C** ≠ **0** is not a product. Digit **D** is independent of **A**, **B**, and **C**. Combinations you can order are listed on the product page; for a special (another clock frequency, …) contact us from there.

Example part numbers

Three worked examples — the same as the wiring drawings later in this guide. Your part number comes from the table above, not from this list.

Scenario	Part number
Minimal duplex, dual supply	**`I2S-001-0000`**
Full passthrough + I²C + external MCLK, 3.3 V in	**`I2S-001-1101`**
On-board 12.288 MHz, 5 V in, no I²C	**`I2S-001-2110`**

3. Power

> **Do not tie grounds or supplies across the barrier.** Even when you supply both sides yourself (**A = 0**), keep **ISO_GND** and noisy **GND** separate, and keep `J1` and `J2` rails separate. Route every signal through the isolators — do not jump a spare control or status line around the barrier. Both sides should sit at about the same voltage; isolation is for noise, not high-voltage stand-off.

Pins **5–6** on each header are that domain's supply. Logic level on a side equals that side's I/O rail — there is no "5 V in, 3.3 V logic" mode. The board **level-shifts** between domains when the two rails differ.

A	0	1	2
Meaning	You supply both sides	**3.3 V** on noisy pin 5 → isolated **3.3 V** out	**5 V** on noisy pin 5 → isolated **3.3 V** out

A = 0: power `J2` (noisy) and `J1` (isolated) from separate regulators. Each side may be 3.3 V or 5 V. Figure 16 is that case: 3.3 V on the CPU / noisy side and 5 V on the codec / isolated side.

A = 1 or **2:** the board generates isolated 3.3 V on pin 5 of `J1` — that pin is an **output**. Do not feed it from the codec supply, and do not parallel the two domains. Isolated I/O stays **3.3 V**. How much current that rail can supply is in §8 (when published). If the codec needs more current than the board can give, power the codec from its own regulator: keep the two **VCC** nets separate, keep **ISO_GND** common with the codec ground (still not across the barrier). Isolated I/O must still be 3.3 V. In that situation **A = 0** is the better order — you are already bringing a second supply. 5 V isolated logic also needs **A = 0**.

4. I2S channels

Count **I2S** wires between the digital side and the audio side — clocks, data, and any extra GPIO you send through the I2S isolator. Omit power, ground, and **I²C** (`SDA` / `SCL` are digit **D**, not this count). Split the count by direction:

- **Toward audio** — e.g. `LRCK`, `BCLK`, DAC data.
- **Back toward digital** — e.g. ADC data, or clocks when the converter is I2S master.

Direction examples (generic, not this board): **Understanding I2S Bus and Audio Isolation**, Figures 1–6 — turul.llc/learn/i2s-bus

Base capacity is **3 + 1** on pins **1–4**. Digit **B** adds pins **7–10**.

Base — pins 1–4 (every board)

Direction	Channels	Pins
Toward audio	**3**	**1, 2, 3**
Back toward digital	**1**	**4**

Assign any net to any pin in the same direction group. Do not swap groups. Typical MCU-master duplex (clocks + DAC data toward the converter, ADC data back) fits **B = 0**.

Digit B — extra I2S

B	Toward audio	Back toward digital
0	Pins **1, 2, 3**	Pin **4**
1, **C = 0**	Pins **1, 2, 3, 7**	Pins **4, 8, 9, 10**
1, **C ≠ 0**	Pins **1, 2, 3, 7**	Pins **4, 8, 9**; pin 10 = on-board reference clock on both headers (frequency from digit **C**)

B = 1 when you need more than **3 + 1**, or when the audio side is I2S clock master. With **B = 0**, pins 7–10 are not routed.

Digit C — pin 10

C	0	1	2, 3, …
Pin 10	Your signal (GPIO, external `MCLK`, …)	On-board **12.288 MHz** on pin 10 of **both** headers (noisy and isolated)	Other on-board frequencies on pin 10 of both headers — not offered yet

Digit **C** applies when **B = 1**. When **C ≠ 0**, the reference clock is on pin 10 of `J1` and `J2`.

5. I²C

Digit **D** is independent of **A**, **B**, and **C**. It only selects whether `SDA` / `SCL` cross the barrier.

D	0	1
Meaning	No I²C path. Leave pins 11–12 unwired.	Isolated `SDA` / `SCL` on pins 11–12

D = 1: Fast Mode Plus (**1 Mbit/s**). **Clock stretching** is supported.

I²C isolation primer: **Understanding I2C Bus Isolation** — turul.llc/learn/i2c-bus

Pull-ups

Each side of the barrier is its own I²C segment — pull-ups are required on **both** sides (on this board or on the MCU / codec board).

On-board **3.3 kΩ** pull-ups use solder jumpers on the component side. Factory default: **all open**.

Jumper	Net
`JP1`	Isolated `SDA`
`JP2`	Isolated `SCL`
`JP3`	Noisy `SDA`
`JP4`	Noisy `SCL`

6. Pin map

Pin *n* on `J2` (noisy / digital) pairs with pin *n* on `J1` (isolated / audio). Pin numbers on the drawing follow PCB layout (1–4, then 5–6 power, then 7–12) — not A/B/C/D order. Coloured bands mark factory options.

Pin	Role
1, 2, 3	Toward audio — always
4	Back toward digital — always
5	**VCC** — noisy: supply input. Isolated: your supply (**A = 0**) or board **3.3 V** out (**A = 1** or **2**)
6	**GND** of that header's domain — do not join the two grounds
7	Toward audio when **B = 1**
8, 9	Back toward digital when **B = 1**
10	When **B = 1** and **C = 0**: back toward digital (your signal). When **C** ≠ **0**: on-board reference clock on **both** headers
11	`SCL` when **D = 1**
12	`SDA` when **D = 1**

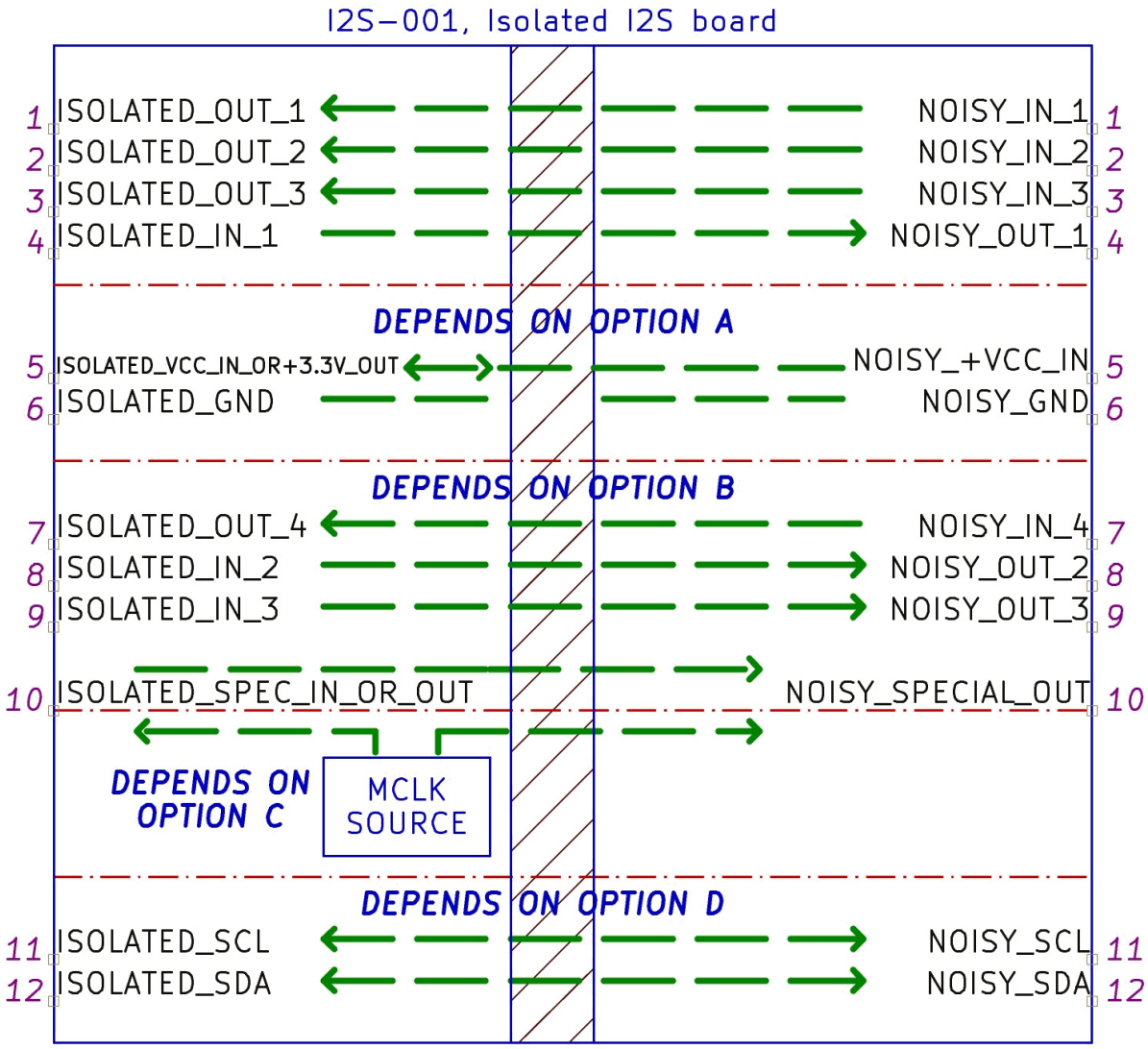


Figure 13. Pin map — passthrough pairs and option bands A–D; generic OUT / IN style labels, not fixed nets.

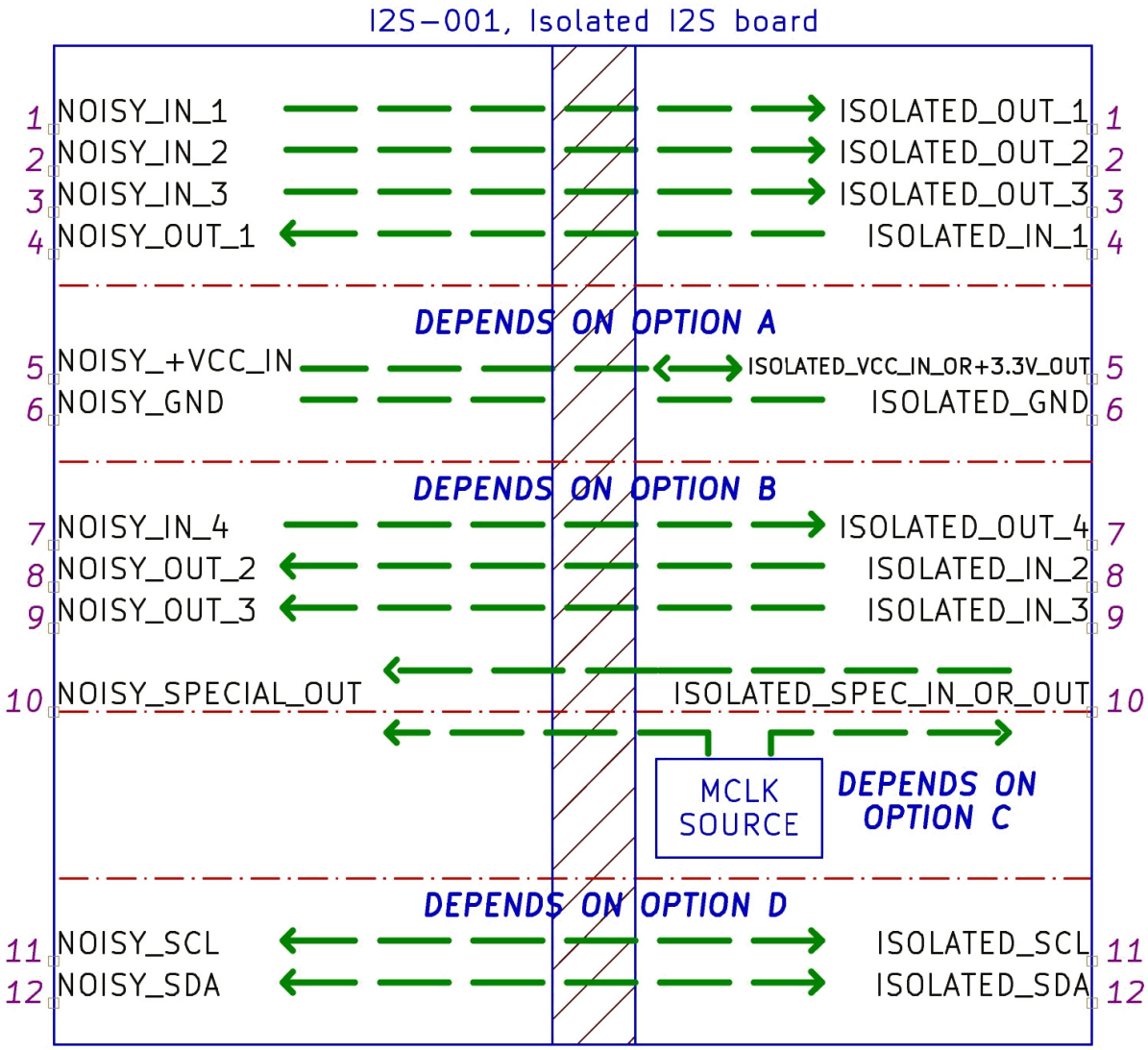
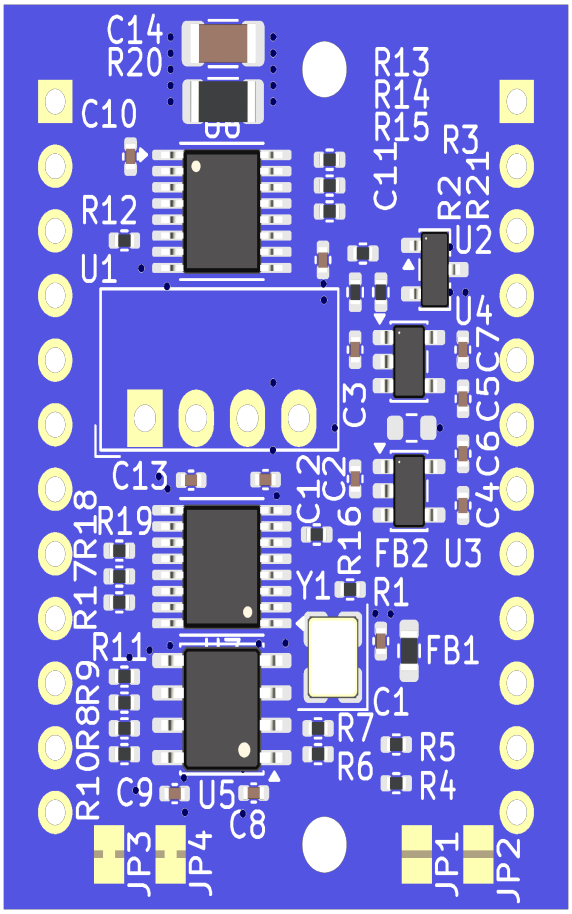
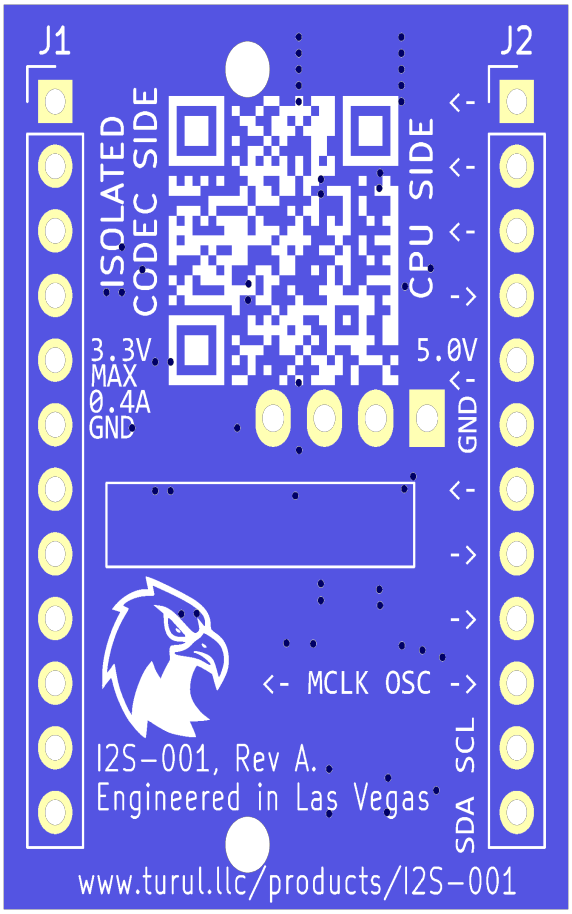


Figure 14. Same map mirrored — pick whichever view matches how you hold the board.



Component side.



Silkscreen side — J1 (isolated) and J2 (CPU).

7. Wiring examples

Three worked examples. Signal-to-pin assignment in each drawing is one possibility — permute within direction groups as in §4. Your part number comes from §2.

> Unused populated inputs: do not leave them floating. Tie the board-side input to ground on *that* domain — **ISO_GND** on J1, **GND** on J2. With **B = 0**, pins 7–10 are not routed; leave them unwired. With **D = 0**, pins 11–12 are not routed. When **C ≠ 0**, pin 10 is the on-board clock — do not treat it as an unused input.

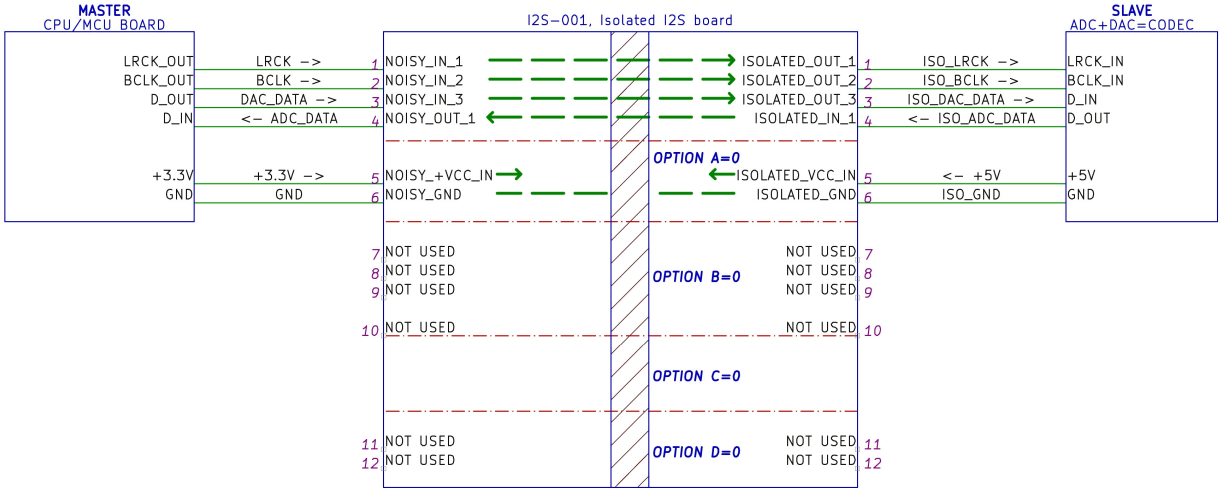


Figure 16. Part number **I2S-001-0000**: MCU clock master duplex — LRCK, BCLK, DAC data on pins **1–3**; ADC data on pin **4**; user dual supply on **5–6** (3.3 V noisy / CPU, 5 V isolated / codec). Pins **7–12** not routed.

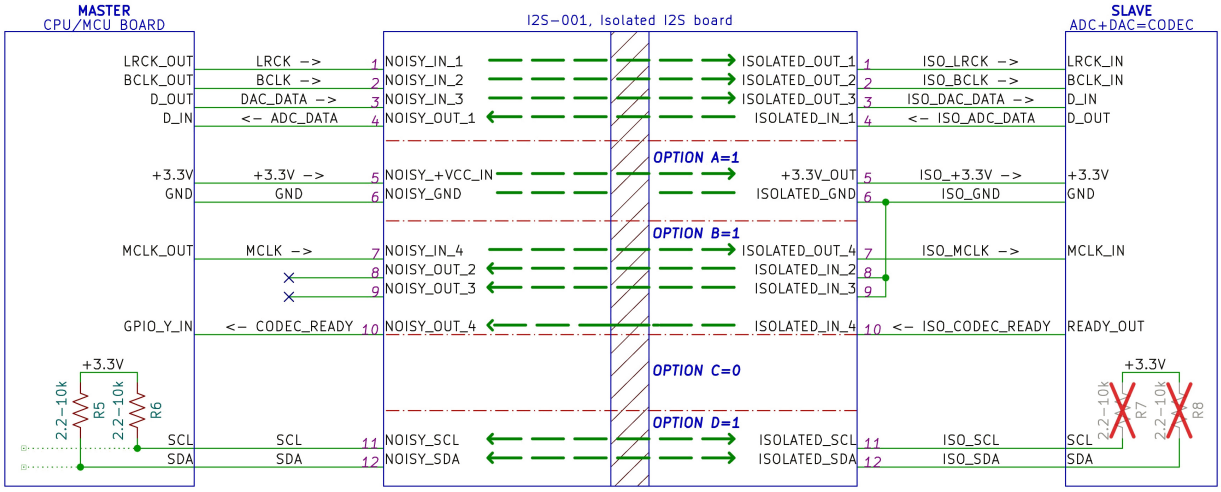


Figure 17. Part number **I2S-001-1101**: MCLK from MCU on pin **7**; CODEC_READY on pin **10**. Unused toward-digital channels **8–9** to **ISO_GND**. I²C on **11–12**.

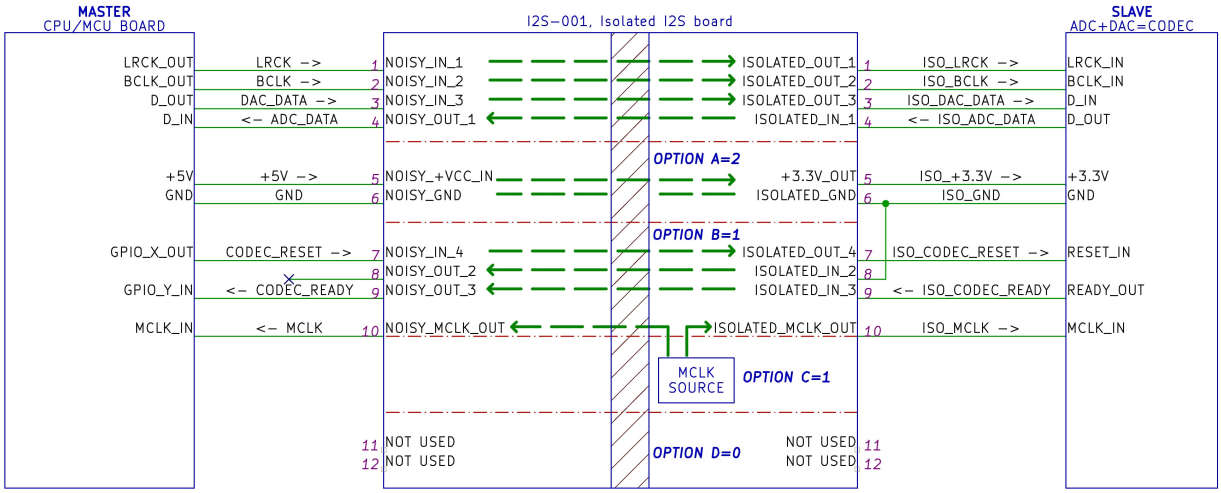
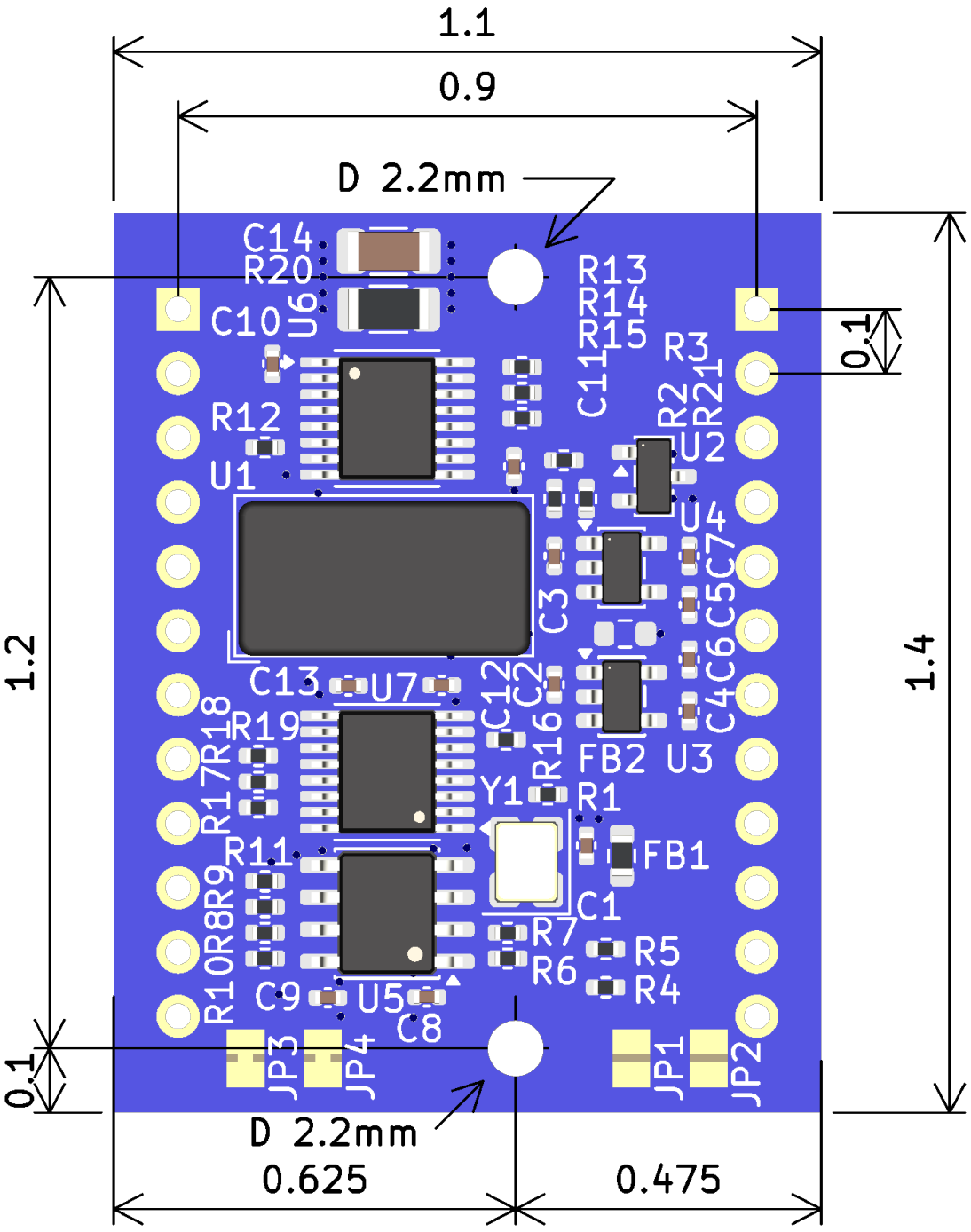


Figure 18. Part number **I2S-001-2110**: on-board reference clock on pin **10** of both headers. RESET on pin **7**; CODEC_READY on pin **9**; unused pin **8** → **ISO_GND**. No I²C.

8. Dimensions & breadboard fit



Board dimensions — inches unless marked mm; 0.1″ pin spacing (2.54 mm breadboard pitch). Fully populated example; your stuffing follows **A**–**D**.

Callout	Meaning
1.1 × 1.4 in **27.9 × 35.6** mm	Board outline (drawing)

0.1″ (2.54 mm)	Center-to-center between neighboring pins in a 12-pin column — standard breadboard pitch
0.9″	Center-to-center between the two header columns
D 2.2 mm	Mounting holes (two). Not on the board centerline — **0.625″** from the left edge, **0.475″** from the right
1.6 mm (0.063 in)	PCB thickness — 2-layer FR4
15 mm (0.59 in)	Assembled height (PCBA)
5 g (0.18 oz)	Weight — board only
60 × 92 × 15 mm **2.36 × 3.62 × 0.59** in	Factory ESD bag; **8 g** with board

Headers are on **2.54 mm (0.1″)** pitch. Span the breadboard center gap with the long edge so `J1` and `J2` sit in opposite columns.

What's in the bag

- The I2S-001 board.
- **Two 1×12 male–male** pin-header strips (2.54 mm / 0.1″) — **not soldered**. You choose length and orientation. If you cut a strip shorter, the board may rock on a breadboard. Other connector styles are on you.
- An adhesive label in the bag — part number, serial, factory-test mark, and a QR code. More fields may be added later.
- Resealable ESD bag.

Identification

The PCB has a silkscreen QR with **no** serial — it opens the product page. Shipping units get an adhesive label over that QR; the label QR includes the serial and opens this site with your unit (ordering options and factory test data). The bag label carries the same serial and the exact part number (`I2S-001-ABCD`).

Silkscreen on the board is not the specification. This guide is.

Electrical

- Logic level on a side equals that side's I/O rail. The board level-shifts between domains.
- **A = 1** or **2:** isolated pin 5 is a 3.3 V **output** — do not feed it. Isolated-rail current capability will be listed here when measured.
- **D = 1:** I²C Fast Mode Plus (**1 Mbit/s**); clock stretching is supported.
- The board has **no overvoltage protection**.
- Isolation is for noise rejection with both sides at roughly the same potential — not a high-voltage barrier. A part's kilovolt-class rating does not apply to the assembled product.

9. Support and warranty

Questions about part numbers or whether your topology fits? Contact links are on the product page.

Warranty does not cover a board destroyed by overvoltage. There is no on-board overvoltage protection — stay within the intended 3.3 V / 5 V rails in §3.